MICROPROCESSOR COMPRISING INPUT MEANS IN THE TEST MODE

Abstract of the Disclosure

A microprocessor includes a counter having a counting input and a reset input. The counting input is coupled to a first terminal of the microprocessor for the selection of an operating mode thereof by application of a predetermined number of pulses to the first terminal. The reset input of the counter is driven by a control signal present on a second terminal of the microprocessor. The control signal is maintained by default at a first logic value ensuring the maintaining at zero of the counter during the initialization period by a circuit internal or external the microprocessor. Immunity against electromagnetic perturbations causing the microprocessor to enter into the test mode is provided.